LP2996-N, LP2996A DDR Termination Regulator

1 Features

- Minimum V_{DDQ}:
  - 1.8 V (LP2996-N)
  - 1.35 V (LP2996A)
- Source and Sink Current
- Low Output Voltage Offset
- No External Resistors Required for Setting Output Voltage
- Linear Topology
- Suspend to Ram (STR) Functionality
- Stable With Ceramic Capacitors With Appropriate ESR
- Low External Component Count
- Thermal Shutdown

2 Applications

- LP2996-N: DDR1 and DDR2 Termination Voltage
- LP2996A: DDR1, DDR2, DDR3, and DDR3L Termination Voltage
- FPGA
- Industrial and Medical PC
- SSTL-2 and SSTL-3 Termination
- HSTL Termination

3 Description

The LP2996-N and LP2996A linear regulators are designed to meet the JEDEC SSTL-2 specifications for termination of DDR-SDRAM. The device also supports DDR2, while LP2996A supports DDR3 and DDR3L VTT bus termination with V_{DDQ} minimum of 1.35 V. The device contains a high-speed operational amplifier to provide excellent response to load transients. The output stage prevents shoot through while delivering 1.5-A continuous current and transient peaks up to 3 A in the application as required for DDR-SDRAM termination. The LP2996-N and LP2996A also incorporate a VSENSE pin to provide superior load regulation and a VREF output as a reference for the chipset and DIMMs.

An additional feature found on the LP2996-N and LP2996A is an active-low shutdown ($\overline{SD}$) pin that provides Suspend To RAM (STR) functionality. When $\overline{SD}$ is pulled low the VTT output will tri-state providing a high impedance output, but VREF remains active. A power savings advantage can be obtained in this mode through lower quiescent current.

TI recommends the LP2998 and LP2998-Q1 devices for automotive applications and DDR applications that require operating at temperatures below zero.

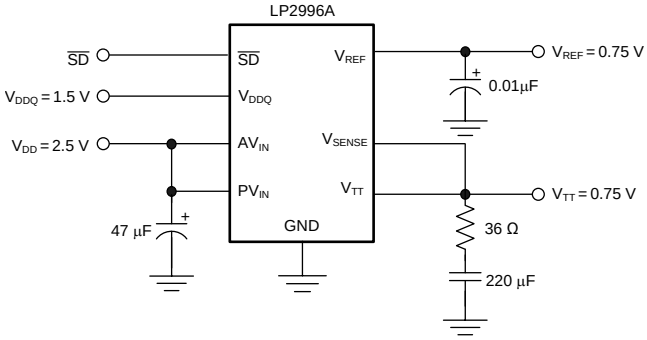
WEBENCH® design tools can be used by application designers to generate, optimize, and simlulate applications using the LP2998 and LP2998-Q1.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LP2996-N	SOIC (8)	4.90 mm x 3.90 mm
LP2996-N, LP2996A	WSON (8)	4.90 mm x 3.90 mm
LP2996-N	WQFN (16)	4.00 mm x 4.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Schematic



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision J (March 2013) to Revision K	Page
• Added *Device Information* table, *Specifications* section, *ESD Ratings* table, *Thermal Information* table, *Feature Description* section, *Device Functional Modes* section, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section	1
• Added LP2996A throughout data sheet	1
• Added DDR3 support throughout data sheet	1
• Deleted Lead temperature (260°C maximum) from *Absolute Maximum Ratings*	5
• Changed Thermal Resistance, $R_{\theta JA}$, values in *Thermal Information* From: 151°C/W To: 119.5°C/W (SOIC), From: 151°C/W To: 56.5°C/W (SO), and From: 151°C/W To: 52.7°C/W (WQFN)	5

Changes from Revision I (March 2013) to Revision J	Page
• Changed layout of National Semiconductor Data Sheet to TI format	1
• Added V_{DDQ} Range	1

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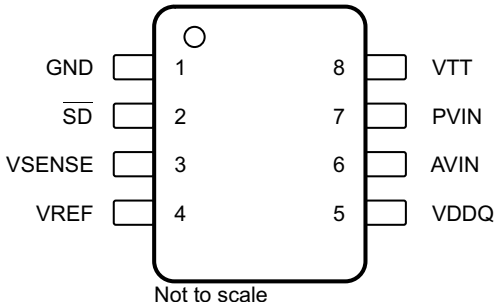
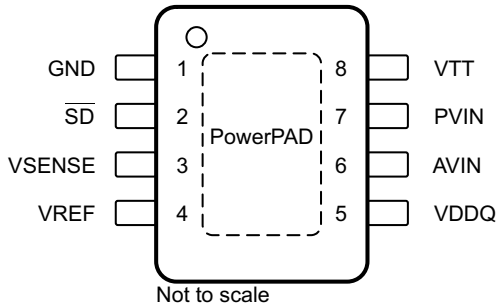
5 Pin Configuration and Functions

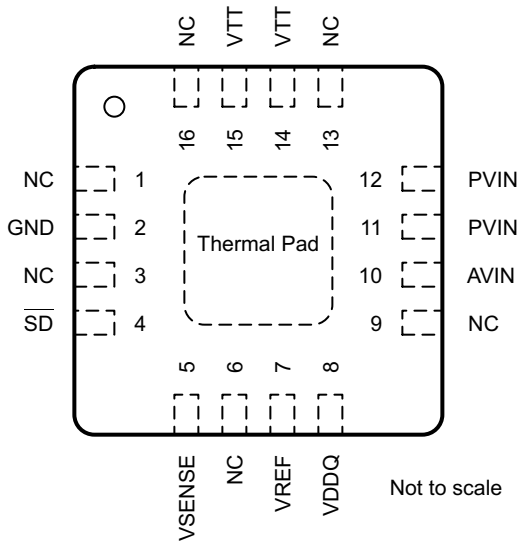
D Package
8-Pin SOIC
Top View



DDA Package
8-Pin SO With PowerPAD
Top View



NHP Package
16-Pin WQFN
Top View



Pin Functions

PIN				I/O	DESCRIPTION
NAME	SO PowerPAD	SOIC	WQFN		
AVIN	6	6	10	I	Analog input pin. AVIN is used to supply all the internal control circuitry. This pin has the capability to work from a supply separate from PVIN depending on the application. For SSTL-2 applications, a good compromise would be to connect the AVIN and PVIN directly together at 2.5 V. This eliminates the requirement for bypassing the two supply pins separately. The only limitation on input voltage selection is that PV_{IN} must be equal to or lower than AV_{IN}.
GND	1	1	2	—	Ground
PVIN	7	7	11, 12	I	Power input pin. PVIN is used exclusively to provide the rail voltage for the output stage used to create VTT. This pin has the capability to work from a supply separate from PVIN depending on the application. Higher voltages on PVIN increases the maximum continuous output current because of output $R_{DS(ON)}$ limitations at voltages close to V_{TT}. The disadvantage of high values of PV_{IN} is that the internal power loss also increases, thermally limiting the design. For SSTL-2 applications, a good compromise would be to connect the AVIN and PVIN directly together at 2.5 V. This eliminates the requirement for bypassing the two supply pins separately. The only limitation on input voltage selection is that PV_{IN} must be equal to or lower than AV_{IN}. TI recommends connecting PVIN to voltage rails equal to or less than 3.3 V to prevent the thermal limit from tripping because of excessive internal power dissipation. If the junction temperature exceeds the thermal shutdown then the part enters a shutdown state identical to the manual shutdown where VTT is tri-stated and VREF remains active.

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Pin Functions (continued)

PIN				I/O	DESCRIPTION
NAME	SO PowerPAD	SOIC	WQFN		
$\overline{SD}$	2	2	4	I	Shutdown. The LP2996-N and LP2996A contain an active low shutdown pin that can be used to tri-state VTT. During shutdown VTT must not be exposed to voltages that exceed AV_{IN}. With the shutdown pin asserted low the quiescent current of the LP2996-N and LP2996A drops, however, VDDQ always maintains its constant impedance of 100 kΩ for generating the internal reference. Therefore, to calculate the total power loss in shutdown, both currents must be considered. See *Thermal Considerations* for more information. The shutdown pin also has an internal pullup current, therefore to turn the part on, the shutdown pin can either be connected to AVIN or left open.
VDDQ	5	5	8	I	Input for internal reference equal to V_{DDQ} / 2. VDDQ is the input used to create the internal reference voltage for regulating V_{TT}. The reference voltage is generated from a resistor divider of two internal 50-kΩ resistors. This ensures that V_{TT} tracks V_{DDQ} / 2 precisely. The optimal implementation of VDDQ is as a remote sense. This can be achieved by connecting VDDQ directly to the 2.5-V rail at the DIMM instead of AVIN and PVIN. This ensures that the reference voltage tracks the DDR memory rails precisely without a large voltage drop from the power lines. For SSTL-2 applications V_{DDQ} is a 2.5-V signal, which creates a 1.25-V termination voltage at VTT. See *Electrical Characteristics* for exact values of V_{TT} over temperature.
VREF	4	4	7	O	Buffered internal reference voltage of V_{DDQ} / 2. VREF provides the buffered output of the internal reference voltage V_{DDQ} / 2. This output must be used to provide the reference voltage for the Northbridge chipset and memory. Because these inputs are typically an extremely high impedance, there must be little current drawn from VREF. For improved performance, an output bypass capacitor can be placed close to the pin to help reduce noise. TI recommends a ceramic capacitor from 0.1 µF to 0.01 µF. This output remains active during the shutdown state and thermal shutdown events for the suspend to RAM functionality.
VSENSE	3	3	5	I	Feedback pin for regulating V_{TT}. The purpose of the sense pin is to provide improved remote load regulation. In most motherboard applications the termination resistors connect to VTT in a long plane. If the output voltage was regulated only at the output of the device then the long trace causes a significant IR drop resulting in a termination voltage lower at one end of the bus than the other. The VSENSE pin can be used to improve this performance by connecting it to the middle of the bus. This provides a better distribution across the entire termination bus. If remote load regulation is not used then the VSENSE pin must still be connected to VTT. Take care when a long VSENSE trace is implemented in close proximity to the memory. Noise pickup in the VSENSE trace can cause problems with precise regulation of V_{TT}. A small 0.1-µF ceramic capacitor placed next to the VSENSE pin can help filter any high frequency signals and preventing errors.
VTT	8	8	14, 15	O	Output voltage for connection to termination resistors. VTT is the regulated output that is used to terminate the bus resistors. It is capable of sinking and sourcing current while regulating the output precisely to V_{DDQ} / 2. The LP2996-N and LP2996A are designed to handle peak transient currents of up to ±3 A with a fast transient response. The maximum continuous current is a function of V_{DD} and can be seen in *Typical Characteristics*. If a transient above the maximum continuous current rating is expected to last for a significant amount of time then the output capacitor must be large enough to prevent an excessive voltage drop. Despite the fact that the device is designed to handle large transient output currents it is not capable of handling these for long durations under all conditions. The reason for this is the standard packages are not able to thermally dissipate the heat as a result of the internal power loss. If large currents are required for longer durations, then ensure that the maximum junction temperature is not exceeded. Proper thermal derating must always be used (see *Thermal Considerations*). If the junction temperature exceeds the thermal shutdown point then VTT tri-states until the part returns below the hysteretic trip-point.
NC	—	—	1, 3, 6, 9, 13, 16	—	No internal connection
Thermal Pad	PowerPAD	—	Thermal Pad	—	Exposed pad thermal connection. Connect to Ground.

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1][2]

	MIN	MAX	UNIT
AVIN to GND	−0.3	6	V
PVIN to GND	–0.3	AV_{IN}	V
Input voltage (VDDQ)[3]	−0.3	6	V
Junction temperature, T_J		150	°C
Storage temperature, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.
(3) VDDQ voltage must be less than 2 × (AVIN – 1) or 6 V, whichever is smaller.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	±1000	V

(1) The human body model is a 100-pF capacitor discharged through a 1.5-kΩ resistor into each pin.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
	AVIN to GND	2.2	5.5	V
	PVIN supply voltage	0	AV_{IN}	V
	$\overline{SD}$ input voltage	0	AV_{IN}	V
T_J	Junction temperature[1]	0	125	°C

(1) At elevated temperatures, devices must be derated based on thermal resistance.

6.4 Thermal Information

THERMAL METRIC		LP2996-N, LP2996A			UNIT
		D (SOIC)	DDA (SO)	NHP (WQFN)	
		8 PINS	8 PINS	16 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	119.5	56.5	52.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	65.3	65.1	50.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	59.8	36.5	30.1	°C/W
ψ_{JT}	Junction-to-top characterization parameter	16.7	15.9	0.7	°C/W
ψ_{JB}	Junction-to-board characterization parameter	59.3	36.5	30.2	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	8.4	9.8	°C/W

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6.5 Electrical Characteristics

Minimum and maximum limits apply over the full operating temperature range (T_J = 0°C to 125°C) and are specified through test, design, or statistical correlation. Typical values represent the most likely parametric norm (T_J = 25°C), and are provided for reference purposes only. Unless otherwise specified, AV_{IN} = PV_{IN} = 2.5 V and V_{DDQ} = 2.5 V.(1)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{REF}	V_{REF} voltage (DDR I)	V_{DD} = V_{DDQ} = 2.3 V		1.135	1.158	1.185	V
		V_{DD} = V_{DDQ} = 2.5 V		1.235	1.258	1.285	
		V_{DD} = V_{DDQ} = 2.7 V		1.335	1.358	1.385	
	V_{REF} voltage (DDR II)	PV_{IN} = V_{DDQ} = 1.7 V		0.837	0.86	0.887	V
		PV_{IN} = V_{DDQ} = 1.8 V		0.887	0.91	0.937	
		PV_{IN} = V_{DDQ} = 1.9 V		0.936	0.959	0.986	
	V_{REF} voltage (DDR III)	PV_{IN} = V_{DDQ} = 1.35 V		0.669	0.684	0.699	V
		PV_{IN} = V_{DDQ} = 1.5 V		0.743	0.758	0.773	
		PV_{IN} = V_{DDQ} = 1.6 V		0.793	0.808	0.823	
Z_{VREF}	V_{REF} output impedance	I_{REF} = –30 to 30 µA			2.5		kΩ
V_{TT}	V_{TT} output voltage (DDR I)(2)	I_{OUT} = 0 A	V_{DD} = V_{DDQ} = 2.3 V	1.12	1.159	1.19	V
			V_{DD} = V_{DDQ} = 2.5 V	1.21	1.259	1.29	
			V_{DD} = V_{DDQ} = 2.7 V	1.32	1.359	1.39	
		I_{OUT} = ±1.5 A	V_{DD} = V_{DDQ} = 2.3 V	1.125	1.159	1.19	
			V_{DD} = V_{DDQ} = 2.5 V	1.225	1.259	1.29	
			V_{DD} = V_{DDQ} = 2.7 V	1.325	1.359	1.39	
	V_{TT} output voltage (DDR II)(2)	I_{OUT} = 0 A, AV_{IN} = 2.5 V	PV_{IN} = V_{DDQ} = 1.7 V	0.822	0.856	0.887	V
			PV_{IN} = V_{DDQ} = 1.8 V	0.874	0.908	0.939	
			PV_{IN} = V_{DDQ} = 1.9 V	0.923	0.957	0.988	
		I_{OUT} = ±0.5 A, AV_{IN} = 2.5 V	PV_{IN} = V_{DDQ} = 1.7 V	0.82	0.856	0.89	
			PV_{IN} = V_{DDQ} = 1.8 V	0.87	0.908	0.94	
			PV_{IN} = V_{DDQ} = 1.9 V	0.92	0.957	0.99	
	V_{TT} output voltage (DDR III)(2)	I_{OUT} = 0 A, AV_{IN} = 2.5 V	PV_{IN} = V_{DDQ} = 1.35 V	0.656	0.677	0.698	V
			PV_{IN} = V_{DDQ} = 1.5 V	0.731	0.752	0.773	
			PV_{IN} = V_{DDQ} = 1.6 V	0.781	0.802	0.823	
		I_{OUT} = 0.2 A, AV_{IN} = 2.5 V, PV_{IN} = V_{DDQ} = 1.35 V		0.667	0.688	0.71	
		I_{OUT} = –0.2 A, AV_{IN} = 2.5 V, PV_{IN} = V_{DDQ} = 1.35 V		0.641	0.673	0.694	
		I_{OUT} = 0.4 A, AV_{IN} = 2.5 V, PV_{IN} = V_{DDQ} = 1.5 V		0.74	0.763	0.786	
		I_{OUT} = –0.4 A, AV_{IN} = 2.5 V, PV_{IN} = V_{DDQ} = 1.5 V		0.731	0.752	0.773	
		I_{OUT} = 0.5 A, AV_{IN} = 2.5 V, PV_{IN} = V_{DDQ} = 1.6 V		0.79	0.813	0.836	
		I_{OUT} = –0.5 A, AV_{IN} = 2.5 V, PV_{IN} = V_{DDQ} = 1.6 V		0.781	0.802	0.823	
VOS_{Vtt}	V_{TT} output voltage offset (V_{REF} – V_{TT}) for DDR I(2)	I_{OUT} = 0 A		–30	0	30	mV
		I_{OUT} = –1.5 A		–30	0	30	
		I_{OUT} = 1.5 A		–30	0	30	
	V_{TT} output voltage offset (V_{REF} – V_{TT}) for DDR II(2)	I_{OUT} = 0 A		–30	0	30	mV
		I_{OUT} = –0.5 A		–30	0	30	
		I_{OUT} = 0.5 A		–30	0	30	
	V_{TT} output voltage offset (V_{REF} – V_{TT}) for DDR III(2)	I_{OUT} = 0 A		–30	0	30	mV
		I_{OUT} = ±0.2 A		–30	0	30	
		I_{OUT} = ±0.4 A		–30	0	30	
		I_{OUT} = ±0.5 A		–30	0	30	
I_Q	Quiescent current(3)	I_{OUT} = 0 A			320	500	µA

(1) V_{DD} is defined as V_{DD} = AV_{IN} = PV_{IN}.
(2) V_{TT} load regulation is tested by using a 10-ms current pulse and measuring V_{TT}.
(3) Quiescent current defined as the current flow into AVIN.

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Electrical Characteristics (continued)

Minimum and maximum limits apply over the full operating temperature range (T_J = 0°C to 125°C) and are specified through test, design, or statistical correlation. Typical values represent the most likely parametric norm (T_J = 25°C), and are provided for reference purposes only. Unless otherwise specified, AV_{IN} = PV_{IN} = 2.5 V and V_{DDQ} = 2.5 V.(1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Z_{VDDQ}	VDDQ input impedance			100		kΩ
I_{SD}	Quiescent current in shutdown(3)	$\overline{SD}$ is low		115	150	µA
I_{Q_SD}	Shutdown leakage current	$\overline{SD}$ is low		2	5	µA
V_{IH}	Minimum shutdown, high level		1.9			V
V_{IL}	Maximum shutdown, low level				0.8	V
I_V	V_{TT} leakage current in shutdown	$\overline{SD}$ is low, V_{TT} = 1.25 V		1	10	µA
I_{SENSE}	V_{SENSE} input current			13		nA
T_{SD}	Thermal shutdown			165		°C
T_{SD_HYS}	Thermal shutdown hysteresis			10		°C

6.6 Typical Characteristics

Unless otherwise specified, AV_{IN} = PV_{IN} = 2.5 V.

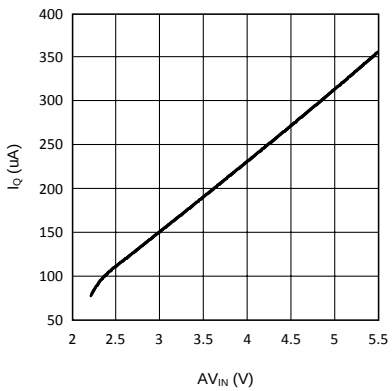


Figure 1. I_Q vs AV_{IN} In Shutdown

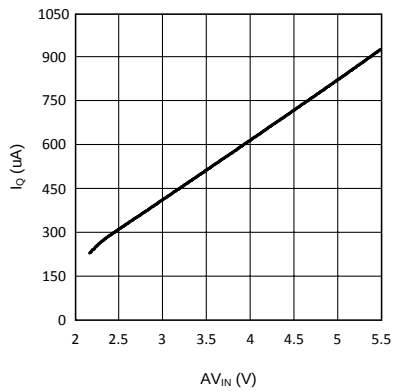


Figure 2. I_Q vs AV_{IN}

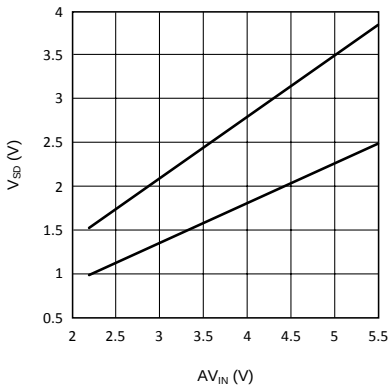


Figure 3. V_{IH} and V_{IL}

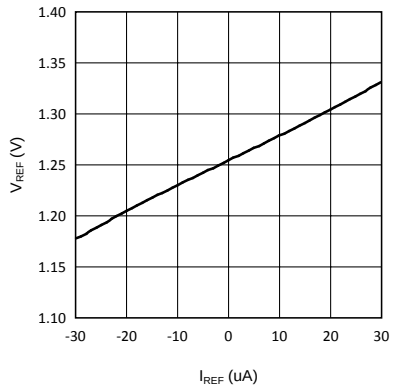


Figure 4. V_{REF} vs I_{REF}

Typical Characteristics (continued)

Unless otherwise specified, $AV_{IN} = PV_{IN} = 2.5$ V.

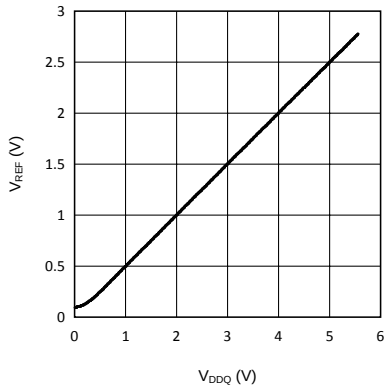


Figure 5. V_{REF} vs V_{DDQ}

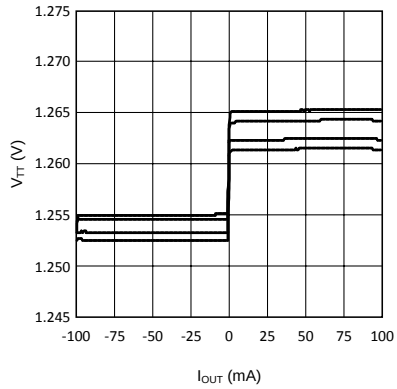


Figure 6. V_{TT} vs I_{OUT}

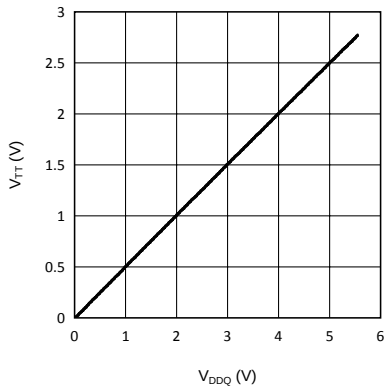


Figure 7. V_{TT} vs V_{DDQ}

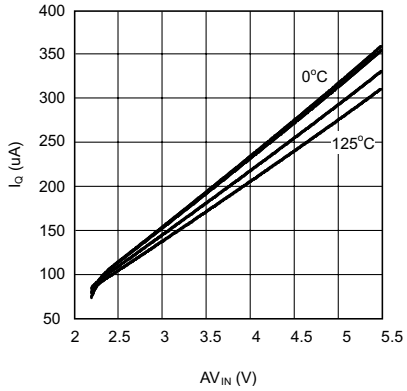


Figure 8. I_Q vs AV_{IN} in Shutdown Temperature

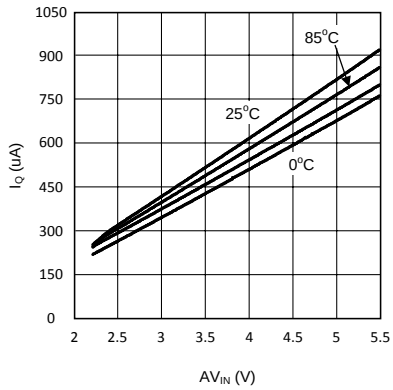
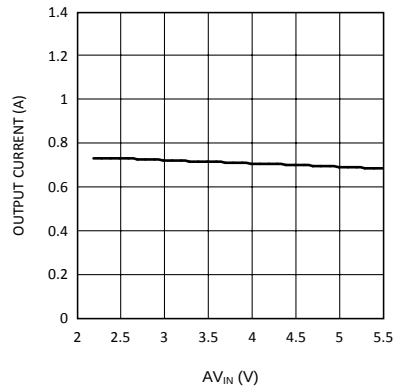


Figure 9. I_Q vs AV_{IN} Temperature



$V_{DDQ} = 2.5$ V $PV_{IN} = 1.8$ V

Figure 10. Maximum Sourcing Current vs AV_{IN}

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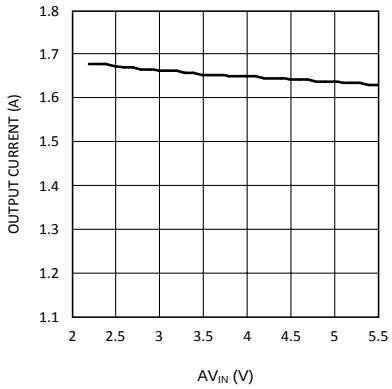
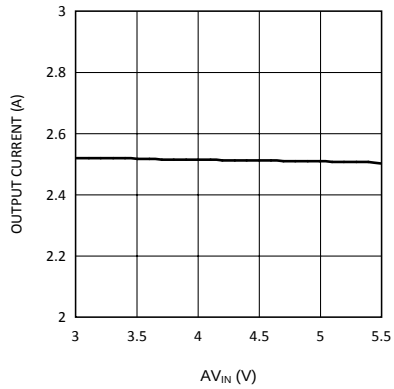
Typical Characteristics (continued)

Unless otherwise specified, AV_{IN} = PV_{IN} = 2.5 V.



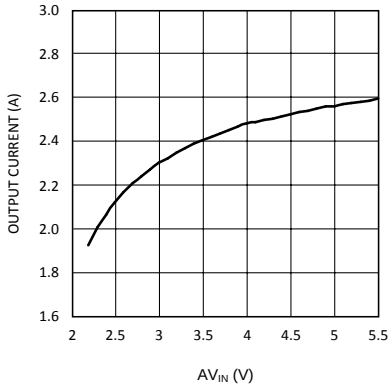
V_{DDQ} = 2.5 V PV_{IN} = 2.5 V

Figure 11. Maximum Sourcing Current vs AV_{IN}



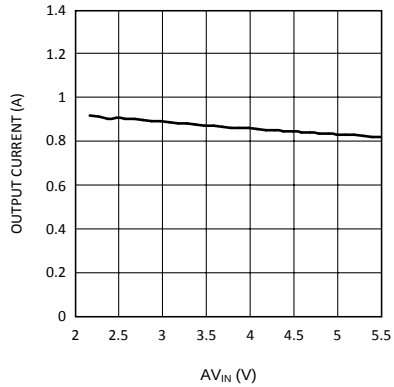
V_{DDQ} = 2.5 V PV_{IN} = 3.3 V

Figure 12. Maximum Sourcing Current vs AV_{IN}



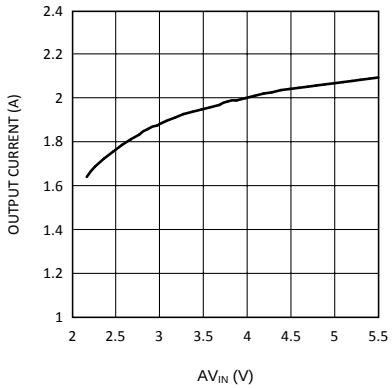
V_{DDQ} = 2.5 V

Figure 13. Maximum Sinking Current vs AV_{IN}



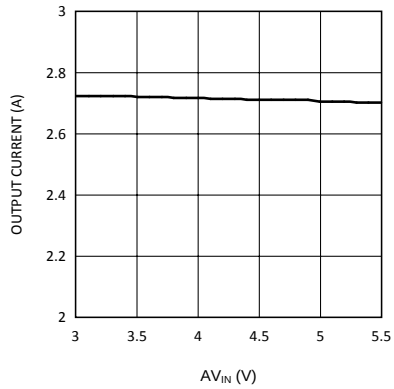
V_{DDQ} = 1.8 V PV_{IN} = 1.8 V

Figure 14. Maximum Sourcing Current vs AV_{IN}



V_{DDQ} = 1.8 V

Figure 15. Maximum Sinking Current vs AV_{IN}



V_{DDQ} = 1.8 V PV_{IN} = 3.3 V

Figure 16. Maximum Sourcing Current vs AV_{IN}

7 Detailed Description

7.1 Overview

The LP2996-N and LP2996A devices can be used to provide a termination voltage for additional logic schemes such as SSTL-3 or HSTL.

Series Stub Termination Logic (SSTL) was created to improve signal integrity of the data transmission across the memory bus. This termination scheme is essential to prevent data error from signal reflections while transmitting at high frequencies encountered with DDR-SDRAM. The most common form of termination is Class II single parallel termination. This involves one R_S series resistor from the chipset to the memory and one R_T termination resistor. Typical values for R_S and R_T are 25 Ω, although these can be changed to scale the current requirements from the LP2996-N or LP2996A. This implementation is shown in Figure 17.

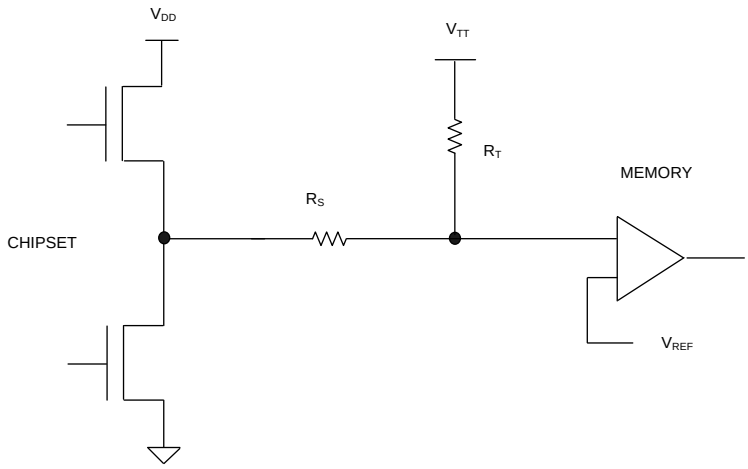
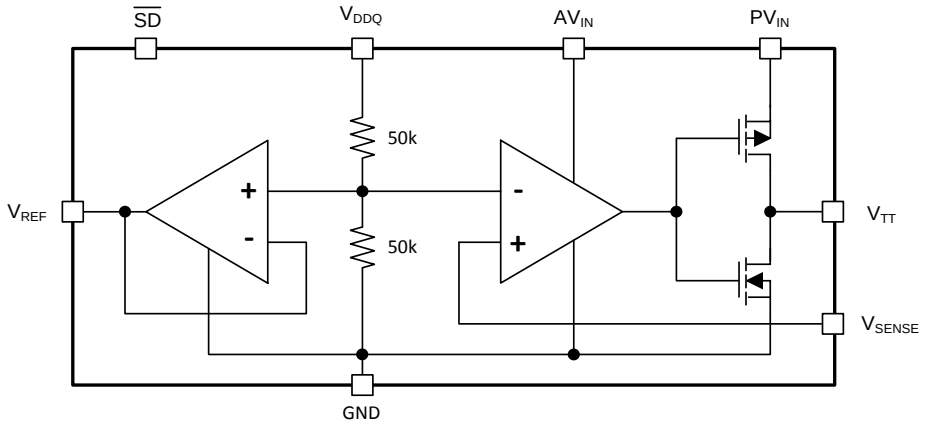


Figure 17. SSTL-Termination Scheme

7.2 Functional Block Diagram



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7.3 Feature Description

The LP2996-N and LP2996A are linear bus termination regulators designed to meet the JEDEC requirements of SSTL-2. The output (V_{TT}) is capable of sinking and sourcing current while regulating the output voltage equal to V_{DDQ} / 2. The output stage is designed to maintain excellent load regulation while preventing shoot through. The LP2996-N and LP2996A also incorporate two distinct power rails that separates the analog circuitry from the power output stage. This allows a split rail approach to be used to decrease internal power dissipation. It also permits the LP2996-N to provide a termination solution for DDR2-SDRAM, while the LP2996A supports DDR3-SDRAM and DDR3L-SDRAM memory. TI recommends the LP2998 and LP2998-Q1 for all DDR applications that require operation at below-zero temperatures.

7.4 Device Functional Modes

7.4.1 Start-Up

During start up when VDDQ is enabled, the error amplifier senses the output voltage is low and drives the pass element hard causing a large inrush current. If this inrush current is too large, the device shuts down and restarts due to the internal current limit. Two solutions to prevent large inrush current during start up:

1. Slow down the slew rate of VDDQ. When the slew rate of VDDQ is fast (approximately 60 µs), the input current can reach over 5 A which exceeds the device's current limit thus causing a restart. If VDDQ start-up slew rate is ≥300 µs, the inrush current can be reduced by 90% limiting the input rush current to less than 500mA.
2. In some cases the system designers have very little to no control over the VDDQ voltage supply slew rate, whether using linear or switching regulators. Some step down voltage regulators do not have soft-start feature. VDDQ voltage source requires only 18 µA current to enable the DDRII termination voltage. Therefore placing an RC filter at VDDQ pin can conveniently increase the output voltage slew rate, allowing a slow rise in capacitor charge current. To keep the VDDQ voltage losses minimum, the resistor value must be chosen carefully. Using a 100-Ω resistor keeps the VDDQ supply voltage losses down to 1.8 mV, because the current through VDDQ is only 18 µA for DDRIII configuration.

See *Limiting DDR Termination Regulators' Inrush Current* (SNVA758) for more information relating to the inrush current during start up.

7.4.2 Normal Operation

The device contains a high-speed operational amplifier to provide excellent response to load transients. The output stage prevents shoot through while delivering 1.5-A continuous current and transient peaks up to 3 A in the application as required for DDR-SDRAM termination. The LP2996-N and LP2996A also incorporate a VSENSE pin to provide superior load regulation and a VREF output as a reference for the chipset and DIMMs. See *Electrical Characteristics* and *Application Information*.

7.4.3 Shutdown

The LP2996-N and LP2996A feature an active-low shutdown (SD) pin that provides Suspend To RAM (STR) functionality. When SD is pulled low, the VTT output tri-states providing a high impedance output, but VREF remains active. A power savings advantage can be obtained in this mode through lower quiescent current. During shutdown, VTT must not be exposed to voltages that exceed AVIN. With the shutdown pin asserted low the quiescent current of the LP2996-N and LP2996A drops, however, VDDQ always maintains its constant impedance of 100 kΩ for generating the internal reference. Therefore, to calculate the total power loss in shutdown, both currents must be considered. The shutdown pin also has an internal pullup current, therefore to turn the part on, the shutdown pin can either be connected to AVIN or left open.

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8 Applications and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The LP2996 has split rails to allow flexibility in powering the device. It has a control circuitry rail (AVIN) and an output power stage rail (PVIN), both separate from the reference voltage input (VDDQ). This allows for different setups which cater to specific requirements such as high current capabilities, lower thermal dissipation, or minimum component count. Because the output is always V_{DDQ} / 2 due to two internal 50-kΩ resistors, the only necessary external components are bypass capacitors.

8.2 Typical Applications

8.2.1 Typical SSTL-2 Application Circuit

This circuit permits termination in a minimum amount of board space and component count. Capacitor selection can be varied depending on the number of lines terminated and the maximum load transient. However, with motherboards and other applications where V_{TT} is distributed across a long plane, it is advisable to use multiple bulk capacitors and addition to high frequency decoupling.

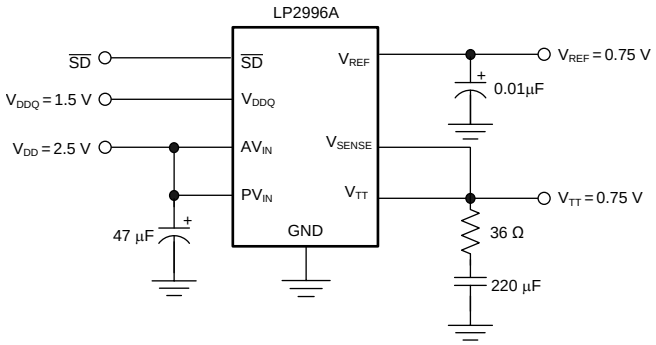

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Figure 18. Typical SSTL-2 Application Circuit Diagram

8.2.1.1 Design Requirements

For this design example, use the parameters listed in Table 1 as the input parameters.

Table 1. Design Parameters

PARAMETER	VALUE
V_{DDQ}	1.5 V
Input to AVIN and PVIN, V_{DD}	2.5 V
V_{REF}	0.75 V
V_{TT}	0.75 V
Input bypass capacitor, C_{IN}	47 µF
Output bypass capacitor, C_{OUT}	220 µF

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8.2.1.2 Detailed Design Procedure

The LP2996 requires voltage be applied to three pins for proper operation: VDDQ, AVIN, and PVIN. VDDQ sets the internal reference voltage and is divided across two 50-kΩ resistors. Therefore, VDDQ must be set at exactly twice the appropriate DDR termination. AVIN powers the internal control circuitry and must be from 2.2 V to 5.5 V. PVIN is the supply for the power output stage and must be larger than or equal to VDDQ while smaller than or equal to AVIN. When picking PVIN, note that smaller values reduce internal power dissipation but reduce the maximum continuous current as well. It is acceptable to tie PVIN to either VDDQ or AVIN to minimize the number of supplies and bypass capacitors required.

To prevent voltage dips on the output, a bypass capacitor must be placed on the VTT line. The size of this capacitor does not affect stability, but larger values improve the transient response and must be sized according to the design requirements. When using ceramic capacitors on the output, large load steps can cause ringing on VTT. Table 2 shows the range of acceptable equivalent series resistance (ESR) that can be added to dampen and improve the response.

Table 2. Approximate ESR Values for VTT Capacitors

VTT CAPACITANCE (µF)	RECOMMENDED ESR (mΩ)
100	50
150	42
220	36
330	30

Another bypass capacitor on PVIN is recommended to keep current spikes from pulling down the input voltage. This is especially important if PVIN and VDDQ are on the same supply. A small 0.01-µF capacitor can be placed on VREF to reduce noise. VSENSE provides a feedback path necessary for regulating the output voltage; Therefore, it must be connected to VTT. If a long VSENSE trace is necessary, a small ceramic capacitor may be required to filter out any high frequency noise picked up from switching I/O signals.

8.2.1.2.1 Input Capacitor

The LP2996-N and LP2996A do not require a capacitor for input stability, but it is recommended for improved performance during large load transients to prevent the input rail from dropping. The input capacitor must be placed as close as possible to the PVIN pin. Several recommendations exist dependent on the application required. A typical value recommended for aluminum electrolytic capacitors is 50 µF. Ceramic capacitors can also be used, a value approximately 10 µF with X5R or better would be an ideal choice. The input capacitance can be reduced if the LP2996-N or LP2996A is placed close to the bulk capacitance from the output of the 2.5-V DC-DC converter. If the two supply rails (AVIN and PVIN) are separated then the 47-µF capacitor must be placed as close to possible to the PVIN rail. An additional 0.1-µF ceramic capacitor can be placed on the AVIN rail to prevent excessive noise from coupling into the device.

8.2.1.2.2 Output Capacitor

The LP2996-N and LP2996A have been designed to be insensitive of output capacitor size or ESR. This allows the flexibility to use any capacitor desired. The choice for output capacitor is determined solely on the application and the requirements for load transient response of V_{TT}. TI recommends the output capacitor be sized above 100 µF with a low ESR for SSTL applications with DDR-SDRAM. The value of ESR is determined by the maximum current spikes expected and the extent at which the output voltage is allowed to droop. Several capacitor options are available on the market and a few of these are discussed: *Aluminum Electrolytics*, *Ceramic Capacitors*, and *Hybrid Capacitors*.

8.2.1.2.2.1 Aluminum Electrolytics

Aluminum electrolytics often only specify impedance at a frequency of 120 Hz, indicating poor high frequency performance. Only aluminum electrolytics that specified an impedance at higher frequencies, from 20 kHz to 100 kHz, must be used for the LP2996-N and LP2996A. To improve the ESR, many aluminum electrolytics may be combined in parallel for an overall reduction. Be aware of the extent at which the ESR changes over temperature. Aluminum electrolytic capacitors' ESR may rapidly increase at cold temperatures.

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8.2.1.2.2.2 Ceramic Capacitors

Ceramic capacitors typically have a low capacitance, from 10 µF to 100 µF, but they have excellent AC performance for bypassing noise due to very low ESR (typically less than 10 mΩ). However, some dielectric types do not have good capacitance characteristics as a function of voltage and temperature. Because of the typically low value of capacitance, TI recommends using ceramic capacitors in parallel with another capacitor such as an aluminum electrolytic. TI recommends dielectric of X5R or better for all ceramic capacitors.

8.2.1.2.2.3 Hybrid Capacitors

Hybrid capacitors offer a large capacitance while maintaining a low ESR. These are the best solution when size and performance are critical, although their cost is typically higher than any other capacitor.

8.2.1.2.2.4 PC Application Considerations

With motherboards and other applications where V_{TT} is distributed across a long plane, it is advisable to use multiple bulk capacitors and addition to high frequency decoupling. Figure 19 shows an example circuit where two bulk output capacitors could be situated at both ends of the V_{TT} plane for optimal placement. Large aluminum electrolytic capacitors are used for their low ESR and low cost.

In most PC applications an extensive amount of decoupling is required because of the long interconnects encountered with the DDR-SDRAM DIMMs mounted on modules. As a result bulk aluminum electrolytic capacitors approximately 1000 µF are typically used.

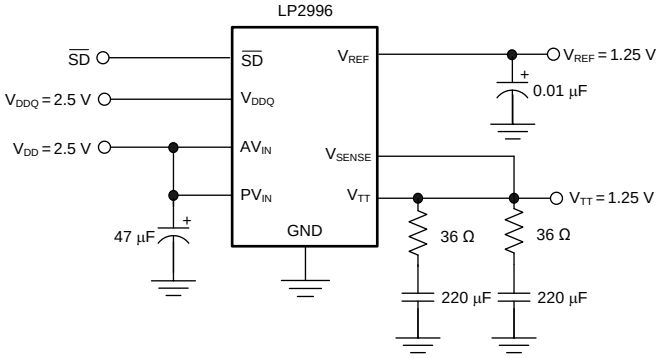

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Figure 19. Typical SSTL-2 Application Circuit for Motherboards

8.2.1.3 Application Curves

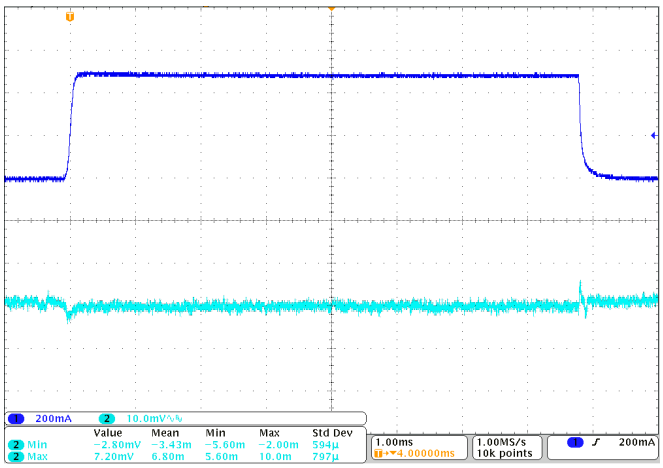

Figure 20. 0.5-A Load Transient With 220-µF V_{TT} Capacitor

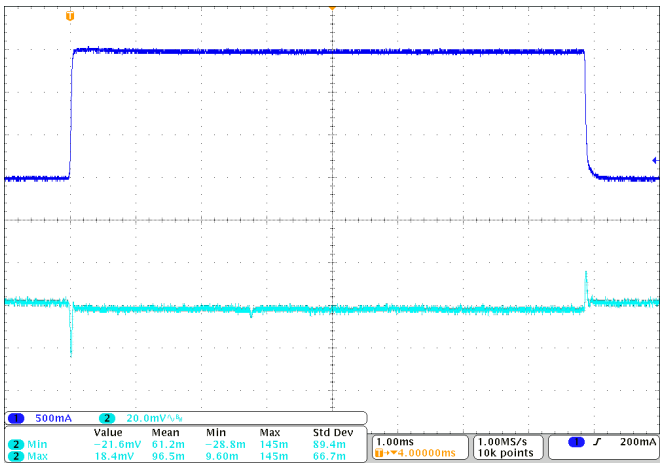

Figure 21. 1.5-A Load Transient With 220-µF V_{TT} Capacitor

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8.2.2 Other Application Circuits

Several different application circuits are shown to illustrate some of the options that are possible in configuring the LP2996-N or LP2996A.

8.2.2.1 SSTL-2 Applications

For the majority of applications that implement the SSTL-2 termination scheme, TI recommends connecting all the input rails to the 2.5-V rail. This provides an optimal trade-off between power dissipation and component count and selection. An example of this circuit can be seen in Figure 22.

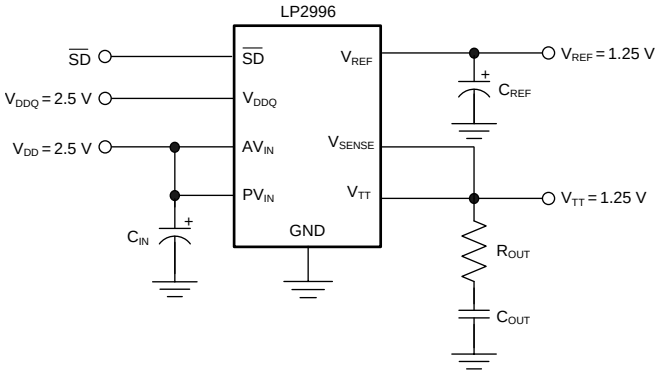

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Figure 22. Recommended SSTL-2 Implementation

If power dissipation or efficiency is a major concern, then the LP2996-N or LP2996A has the ability to operate on split power rails. The output stage (PVIN) can be operated on a lower rail such as 1.8 V and the analog circuitry (AVIN) can be connected to a higher rail such as 2.5 V, 3.3 V, or 5 V. This allows the internal power dissipation to be lowered when sourcing current from VTT. The disadvantage of this circuit is that the maximum continuous current is reduced because of the lower rail voltage, although it is adequate for all motherboard SSTL-2 applications. Increasing the output capacitance can also help if periods of large load transients are encountered.

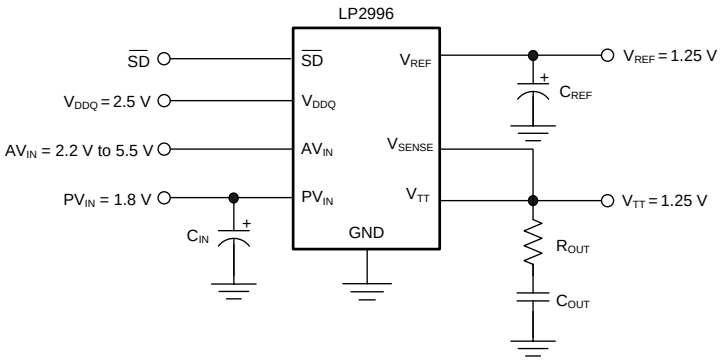

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Figure 23. Lower Power Dissipation SSTL-2 Implementation

The third option for SSTL-2 applications in the situation that a 1.8-V rail is not available and it is not desirable to use 2.5 V, is to connect the LP2996-N or LP2996A power rail to 3.3 V. In this situation AVIN is limited to operation on the 3.3-V or 5-V rail as PVIN can never exceed AVIN. This configuration has the ability to provide the maximum continuous output current at the downside of higher thermal dissipation. Prevent the device from experiencing large current levels which cause the junction temperature to exceed the maximum. Because of this risk, TI recommends not supplying the output stage with a voltage higher than a nominal 3.3-V rail.

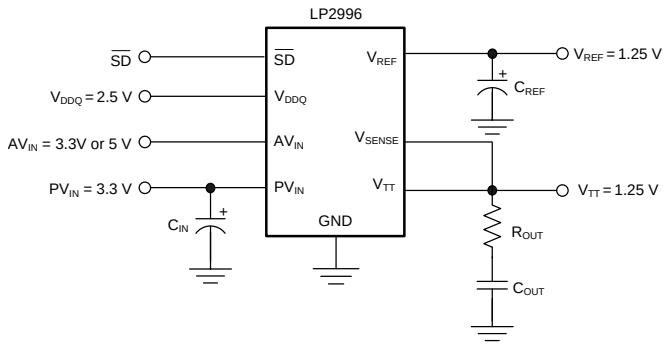

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Figure 24. SSTL-2 Implementation with Higher Voltage Rails

8.2.2.2 DDR-II Applications

With the separate VDDQ pin and an internal resistor divider it is possible to use the LP2996-N and LP2996A in applications utilizing DDR-II memory. Figure 25 and Figure 26 show implementations of recommended circuit configurations for DDR-II applications. The output stage is connected to the 1.8-V rail and the AVIN pin can be connected to either a 3.3-V or 5-V rail. TI recommends the LP2996A, LP2998, or LP2998-Q1 for DDR-III and DDR-III low power designs.

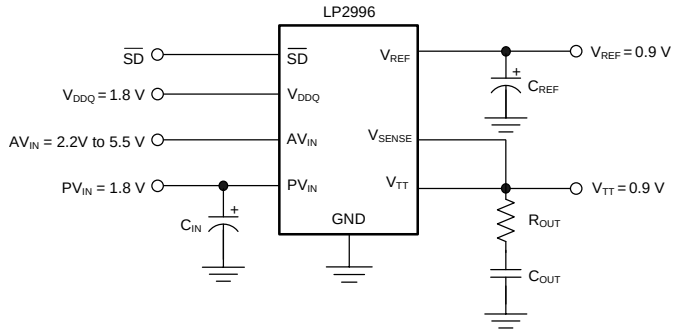

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Figure 25. Recommended DDR-II Termination

If it is not desirable to use the 1.8-V rail it is possible to connect the output stage to a 3.3-V rail. Take care not to exceed the maximum junction temperature as the thermal dissipation increases with lower VTT output voltages. For this reason, TI does not recommend powering PVIN from a rail higher than the nominal 3.3 V. The advantage of this configuration is that it has the ability to source and sink a higher maximum continuous current.

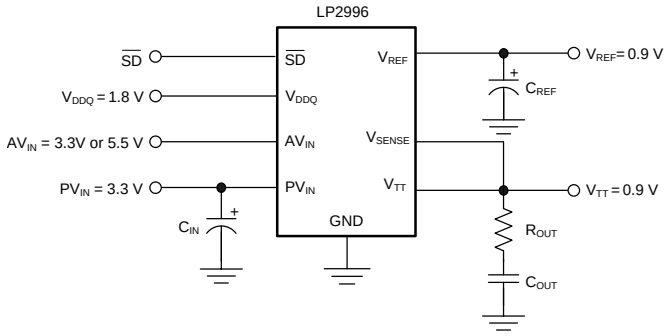

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Figure 26. DDR-II Termination with Higher Voltage Rails

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8.2.2.3 DDR-III Applications

With the separate VDDQ pin and an internal resistor divider it is possible to use the LP2996A in applications utilizing DDR-III memory. The output stage is connected to the 1.5-V rail and the AVIN pin can be connected to a 2.2-V to 5.5-V rail.

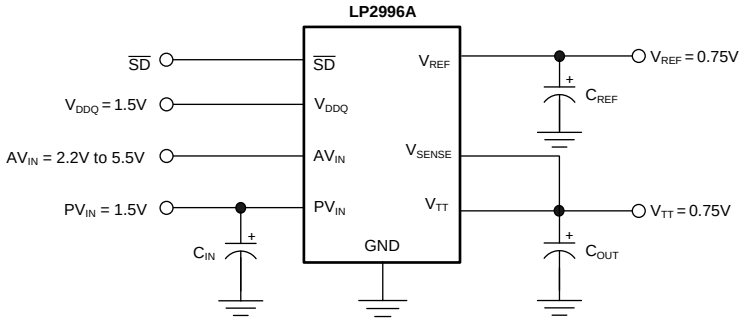

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Figure 27. Recommended DDR-III Termination Using the LP2996A

If it is not desirable to use the 1.5-V to 2.5-V rail it is possible to connect the output stage to a 3.3-V rail. Do not exceed the maximum junction temperature as the thermal dissipation increases with lower V_{TT} output voltages. For this reason, TI recommends not to power PVIN off a rail higher than the nominal 3.3-V. The advantage of this configuration is that it has the ability to source and sink a higher maximum continuous current.

8.2.3 Level Shifting

If standards other than SSTL-2 are required, such as SSTL-3, it may be necessary to use a different scaling factor than V_{DDQ} / 2 for regulating the output voltage. Several options are available to scale the output to any voltage required. One method is to level shift the output by using feedback resistors from VTT to the VSENSE pin. This is shown in Figure 28 and Figure 29. Figure 28 shows how to use two resistors to level shift V_{TT} above the internal reference voltage of V_{DDQ} / 2. Calculate the exact voltage at VTT with Equation 1.

$$V_{TT} = \frac{V_{DDQ}}{2} \times \left(1 + \frac{R1}{R2}\right) \tag{1}$$

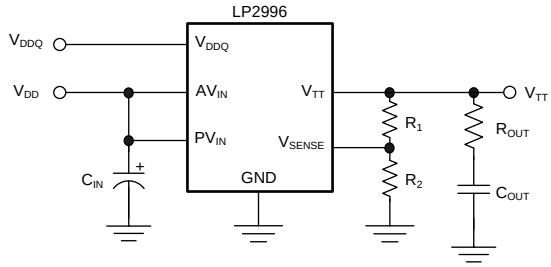

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Figure 28. Increasing V_{TT} by Level Shifting

Conversely, the R2 resistor can be placed between VSENSE and VDDQ to shift the VTT output lower than the internal reference voltage of V_{DDQ} / 2. Equation 2 shows the relation of V_{TT} to the resistors.

$$V_{TT} = \frac{V_{DDQ}}{2} \times \left(1 - \frac{R1}{R2}\right) \tag{2}$$

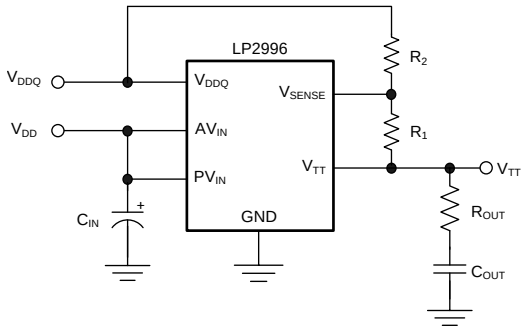

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Figure 29. Decreasing V_{TT} by Level Shifting

8.2.4 HSTL Applications

The LP2996-N and LP2996A can be easily adapted for HSTL applications by connecting VDDQ to the 1.5-V rail. This produces a VTT and VREF voltage of approximately 0.75 V for the termination resistors. AVIN and PVIN must be connected to a 2.5-V rail for optimal performance.

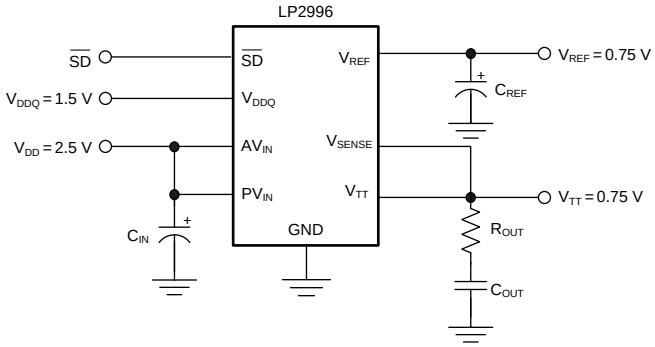

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Figure 30. HSTL Application

8.2.5 QDR Applications

Quad data rate (QDR) applications use multiple channels for improved memory performance. However, this increase in bus lines increases the current levels required for termination. TI recommends using a dedicated LP2996-N or LP2996A for each channel to terminate multiple channels. This simplifies layout and reduces the internal power dissipation for each regulator. Separate VREF signals can be used for each DIMM bank from the corresponding regulator with the chipset reference provided by a local resistor divider or one of the LP2996-N or LP2996A signals. Because V_{REF} and V_{TT} are expected to track and the part to part variations are minor, there must be little difference between the reference signals of each device.

9 Power Supply Recommendations

There are several recommendations for the LP2996-N and LP2996A input power supply. Although not required, TI recommends an input capacitor for improved performance during large load transients to prevent the input rail from dropping. The input capacitor must be placed as close as possible to the PVIN pin.

A typical value recommended for aluminum electrolytic capacitors is 50 µF. Ceramic capacitors can also be used, a value approximately 10 µF with X5R or better would be an ideal choice. The input capacitance can be reduced if the LP2996-N or LP2996A is placed close to the bulk capacitance from the output of the 2.5-V DC-DC converter. If the two supply rails (AVIN and PVIN) are separated then the 47-µF capacitor must be placed as close to possible to the PVIN rail. An additional 0.1-µF ceramic capacitor can be placed on the AVIN rail to prevent excessive noise from coupling into the device.

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10 Layout

10.1 Layout Guidelines

- The input capacitor for the power rail must be placed as close as possible to the PVIN pin.
- VSENSE must be connected to the VTT termination bus at the point where regulation is required. For motherboard applications an ideal location would be at the center of the termination bus.
- VDDQ can be connected remotely to the VDDQ rail input at either the DIMM or the chipset. This provides the most accurate point for creating the reference voltage.
- For improved thermal performance excessive top side copper can be used to dissipate heat from the package. Numerous vias from the ground connection to the internal ground plane helps. Additionally these can be placed underneath the package if manufacturing standards permit.
- Take care when routing the V_{SENSE} trace to avoid noise pickup from switching I/O signals. A 0.1-µF ceramic capacitor placed close to VSENSE can also be used to filter any unwanted high frequency signal. This can be an issue especially if long VSENSE traces are used.
- VREF must be bypassed with a 0.01-µF or 0.1-µF ceramic capacitor for improved performance. This capacitor must be placed as close as possible to the VREF pin.

10.2 Layout Examples

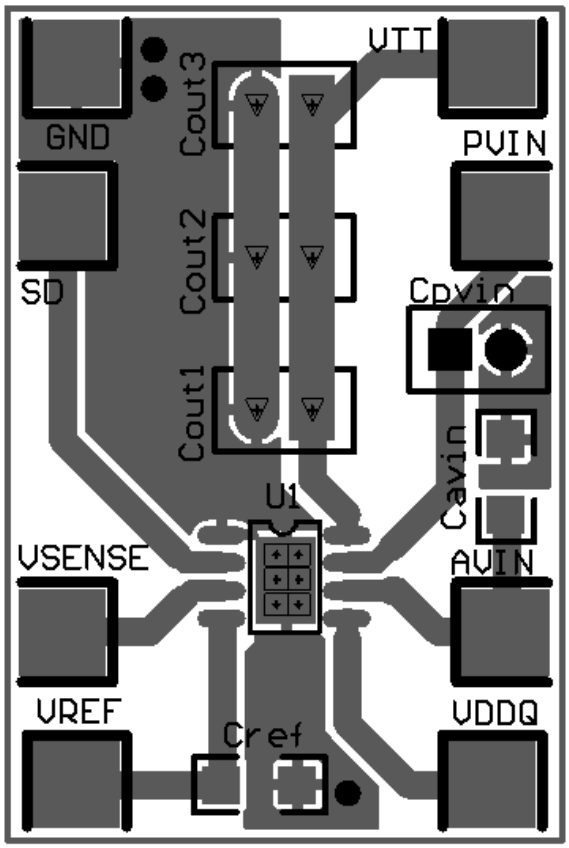

Figure 31. Layout Example of the SO PowerPAD Package (Top Layer)

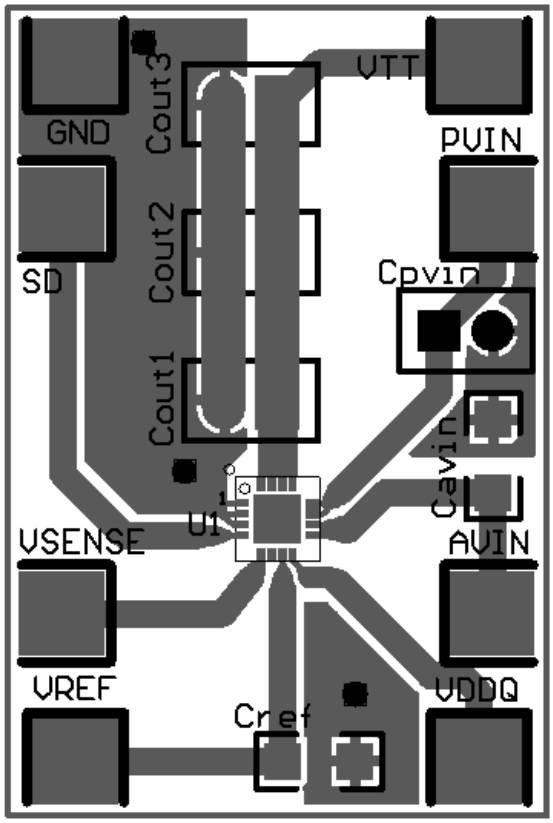

Figure 32. Layout Example of the WQFN Package (Top Layer)

10.3 Thermal Considerations

Because the LP2996-N and LP2996A are linear regulators, any current flow from VTT results in internal power dissipation generating heat. To prevent damaging the part from exceeding the maximum allowable junction temperature, derate the part according to the maximum expected ambient temperature and power dissipation. The maximum allowable internal temperature rise ($T_{R(MAX)}$) can be calculated with Equation 3 given the maximum ambient temperature ($T_{A(MAX)}$) of the application and the maximum allowable junction temperature ($T_{J(MAX)}$).

$$T_{R(MAX)} = T_{J(MAX)} - T_{A(MAX)} \quad (3)$$

From this equation, the maximum power dissipation ($P_{D(MAX)}$) of the part can be calculated with Equation 4.

$$P_{D(MAX)} = T_{R(MAX)} / R_{\theta JA} \quad (4)$$

The $R_{\theta JA}$ of the LP2996-N and LP2996A is dependent on several variables: the package used; the thickness of copper; the number of vias and the airflow. For instance, the $R_{\theta JA}$ of the SOIC is 163°C/W with the package mounted to a standard 8×4 2-layer board with 1-oz copper, no airflow, and 0.5-W dissipation at room temperature. This value can be reduced to 151.2°C/W by changing to a 3×4 board with 2-oz copper that is the JEDEC standard. Figure 33 shows how the $R_{\theta JA}$ varies with airflow for the two boards mentioned.

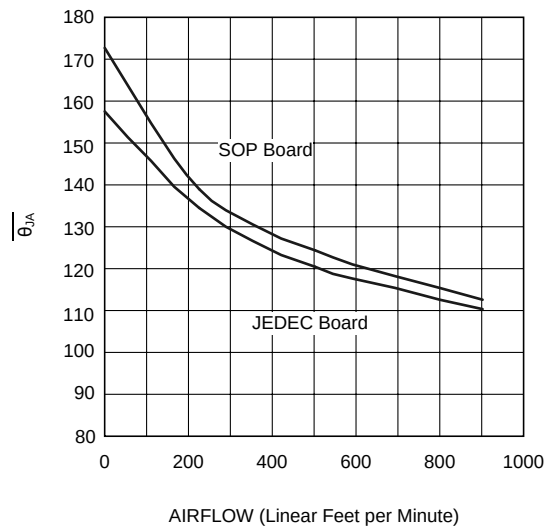

Figure 33. $R_{\theta JA}$ vs Airflow (SOIC)

Additional improvements can be made by the judicious use of vias to connect the part and dissipate heat to an internal ground plane. Using larger traces and more copper on the top side of the board can also help. With careful layout, it is possible to reduce the $R_{\theta JA}$ further than the nominal values shown in Figure 33

Layout is also extremely critical to maximize the output current with the WQFN package. By simply placing vias under the thermal pad, the $R_{\theta JA}$ can be lowered significantly. Figure 34 shows the WQFN thermal data when placed on a 4-layer JEDEC board with copper thickness of 0.5 oz, 1 oz, 1 oz, and 0.5 oz (respectively). The number of vias with a pitch of 1.27 mm is increased to the maximum of 4, where a $R_{\theta JA}$ of 50.41°C/W can be obtained. Via wall thickness for this calculation is 0.036 mm for 1-oz copper.

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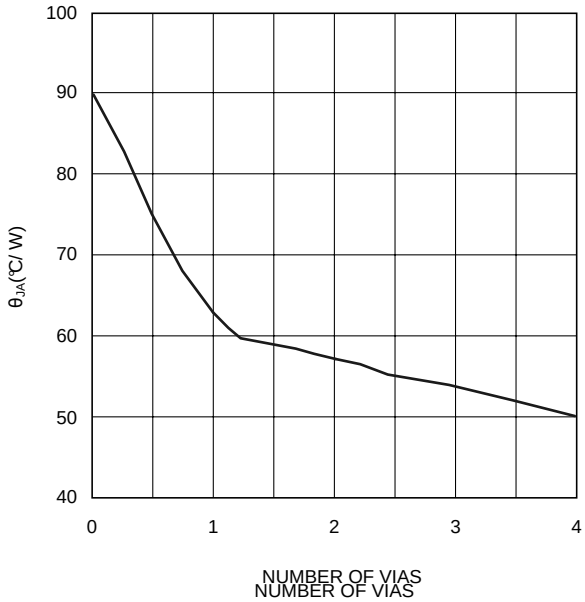
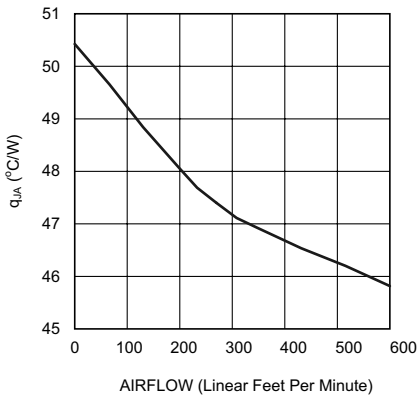
Thermal Considerations (continued)



4-layer JEDEC board

Figure 34. WQFN-16 $R_{\theta JA}$ vs Number of Vias

Additional improvements in lowering the $R_{\theta JA}$ can be achieved with a constant airflow across the package. Maintaining the same conditions as above and utilizing the 2×2 via array, Figure 35 shows how the $R_{\theta JA}$ varies with airflow.



JEDEC board with 4 vias

Figure 35. $R_{\theta JA}$ vs Airflow Speed

Thermal Considerations (continued)

Optimizing the $R_{\theta JA}$ and placing the device in a section of a board exposed to lower ambient temperature allows the part to operate with higher power dissipation. The internal power dissipation can be calculated by summing the three main sources of loss: output current at VTT, either sinking or sourcing, and quiescent current at AVIN and VDDQ. During the active state, when the shutdown pin ($\overline{SD}$) is not held low, the total internal power dissipation can be calculated with Equation 5.

$$P_D = P_{AVIN} + P_{VDDQ} + P_{VTT}$$

where

- $P_{AVIN} = I_{AVIN} \times V_{AVIN}$
- $P_{VDDQ} = V_{VDDQ} \times I_{VDDQ} = V_{VDDQ2} \times R_{VDDQ}$ (5)

To calculate the maximum power dissipation at VTT both conditions (sinking and sourcing current) at VTT must be examined. Although only one equation is added into the total, because VTT cannot source and sink current simultaneously.

Calculate sinking with Equation 6.

$$P_{VTT} = V_{VTT} \times I_{LOAD} \quad (6)$$

Or calculate sourcing with Equation 7.

$$P_{VTT} = (V_{PVIN} - V_{VTT}) \times I_{LOAD} \quad (7)$$

The power dissipation of the LP2996-N and LP2996A can also be calculated during the shutdown state. During this condition the output (VTT) is tri-stated; Therefore, that term in the power equation disappears as it cannot sink or source any current, and leakage is negligible. The only losses during shutdown are the reduced quiescent current at AVIN and the constant impedance that is seen at the VDDQ pin.

$$P_D = P_{AVIN} + P_{VDDQ}$$

where

- $P_{AVIN} = I_{AVIN} \times V_{AVIN}$
- $P_{VDDQ} = V_{VDDQ} \times I_{VDDQ} = V_{VDDQ2} \times R_{VDDQ}$ (8)

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11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

For related documentation see the following:

Limiting DDR Termination Regulators' Inrush Current (SNVA758)

11.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 3. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
LP2996-N	Click here	Click here	Click here	Click here	Click here
LP2996A	Click here	Click here	Click here	Click here	Click here

11.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.4 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.5 Trademarks

E2E is a trademark of Texas Instruments.
WEBENCH is a registered trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LP2996AMR/NOPB	ACTIVE	SO PowerPAD	DDA	8	95	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR	0 to 125	LP2996 AMR	Samples
LP2996AMRE/NOPB	ACTIVE	SO PowerPAD	DDA	8	250	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR	0 to 125	LP2996 AMR	Samples
LP2996AMRX/NOPB	ACTIVE	SO PowerPAD	DDA	8	2500	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR	0 to 125	LP2996 AMR	Samples
LP2996LQ/NOPB	ACTIVE	WQFN	NHP	16	1000	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR	0 to 125	L00006B	Samples
LP2996LQX/NOPB	ACTIVE	WQFN	NHP	16	4500	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR	0 to 125	L00006B	Samples
LP2996M	NRND	SOIC	D	8	95	TBD	Call TI	Call TI	0 to 125	2996M	
LP2996M/NOPB	ACTIVE	SOIC	D	8	95	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	0 to 125	2996M	Samples
LP2996MR	NRND	SO PowerPAD	DDA	8	95	TBD	Call TI	Call TI	0 to 125	LP2996	
LP2996MR/NOPB	ACTIVE	SO PowerPAD	DDA	8	95	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR	0 to 125	LP2996	Samples
LP2996MRX	NRND	SO PowerPAD	DDA	8	2500	TBD	Call TI	Call TI	0 to 125	LP2996	
LP2996MRX/NOPB	ACTIVE	SO PowerPAD	DDA	8	2500	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR	0 to 125	LP2996	Samples
LP2996MX/NOPB	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	0 to 125	2996M	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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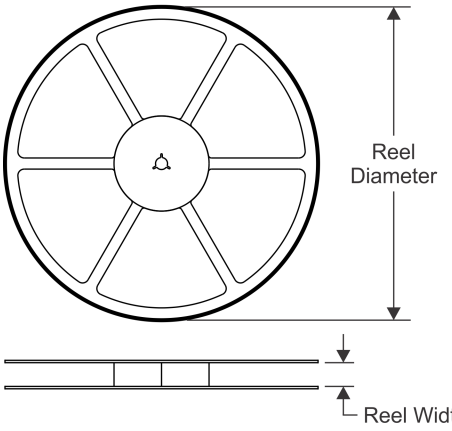
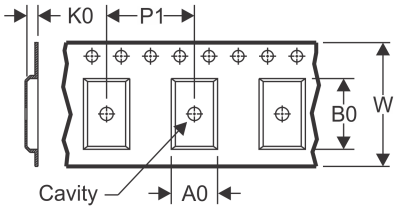
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

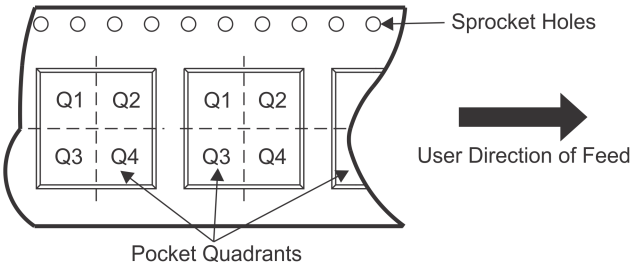


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

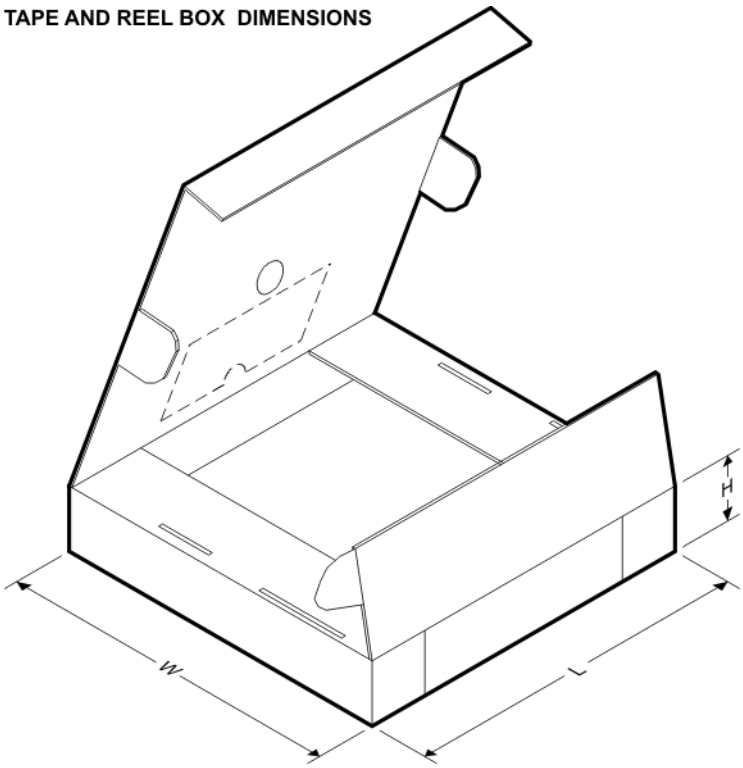
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LP2996AMRE/NOPB	SO Power PAD	DDA	8	250	178.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LP2996AMRX/NOPB	SO Power PAD	DDA	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LP2996LQ/NOPB	WQFN	NHP	16	1000	178.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1
LP2996LQX/NOPB	WQFN	NHP	16	4500	330.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1
LP2996MRX	SO Power PAD	DDA	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LP2996MRX/NOPB	SO Power PAD	DDA	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LP2996MX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1

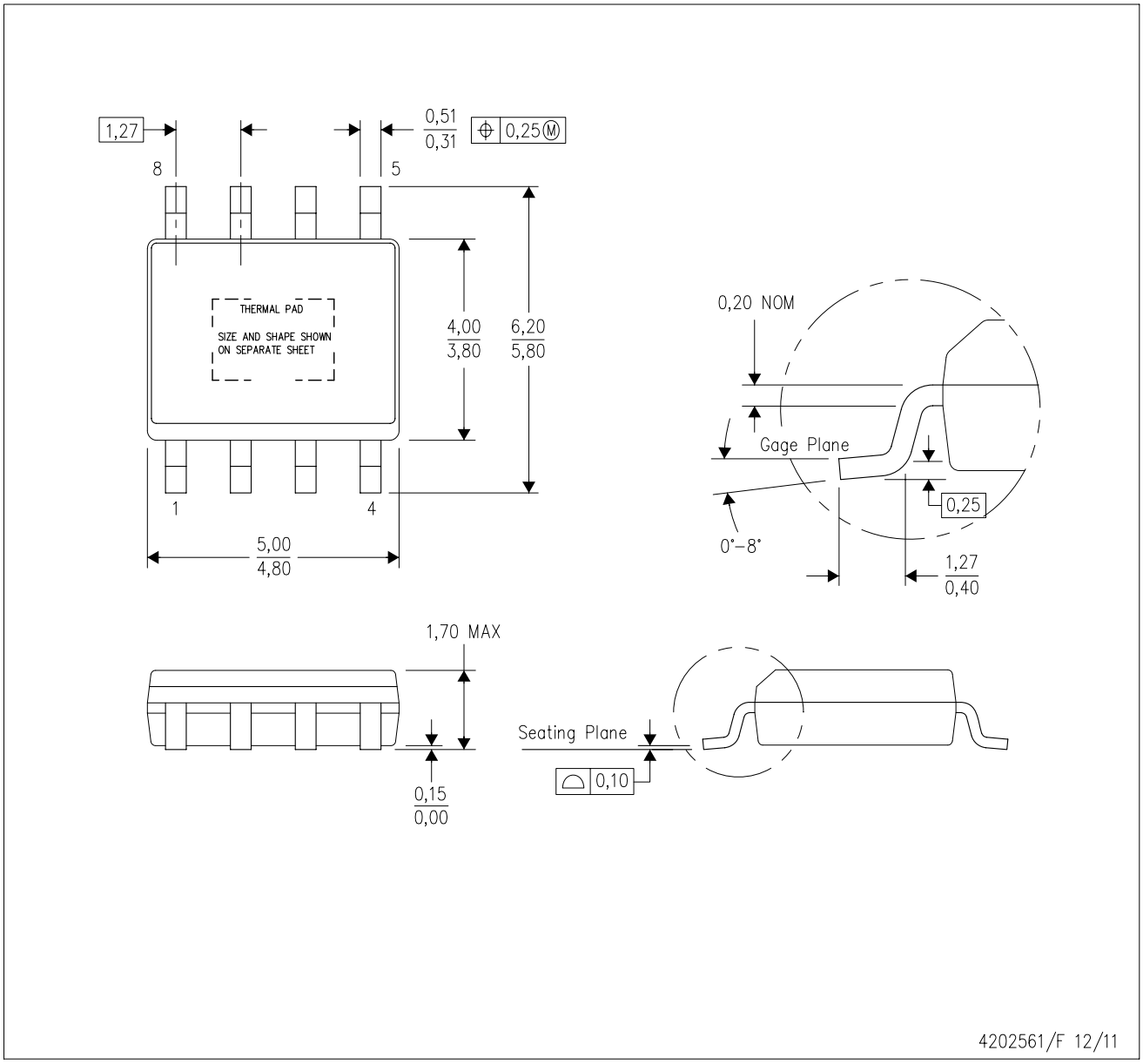
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LP2996AMRE/NOPB	SO PowerPAD	DDA	8	250	210.0	185.0	35.0
LP2996AMRX/NOPB	SO PowerPAD	DDA	8	2500	367.0	367.0	35.0
LP2996LQ/NOPB	WQFN	NHP	16	1000	210.0	185.0	35.0
LP2996LQX/NOPB	WQFN	NHP	16	4500	367.0	367.0	35.0
LP2996MRX	SO PowerPAD	DDA	8	2500	367.0	367.0	35.0
LP2996MRX/NOPB	SO PowerPAD	DDA	8	2500	367.0	367.0	35.0
LP2996MX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0

DDA (R-PDSO-G8) PowerPAD™ PLASTIC SMALL-OUTLINE



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5–1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. This package complies to JEDEC MS-012 variation BA

PowerPAD is a trademark of Texas Instruments.

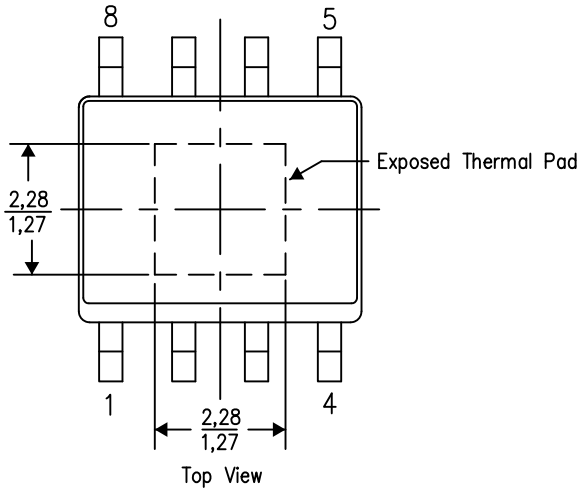
DDA (R-PDSO-G8) PowerPAD™ PLASTIC SMALL OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



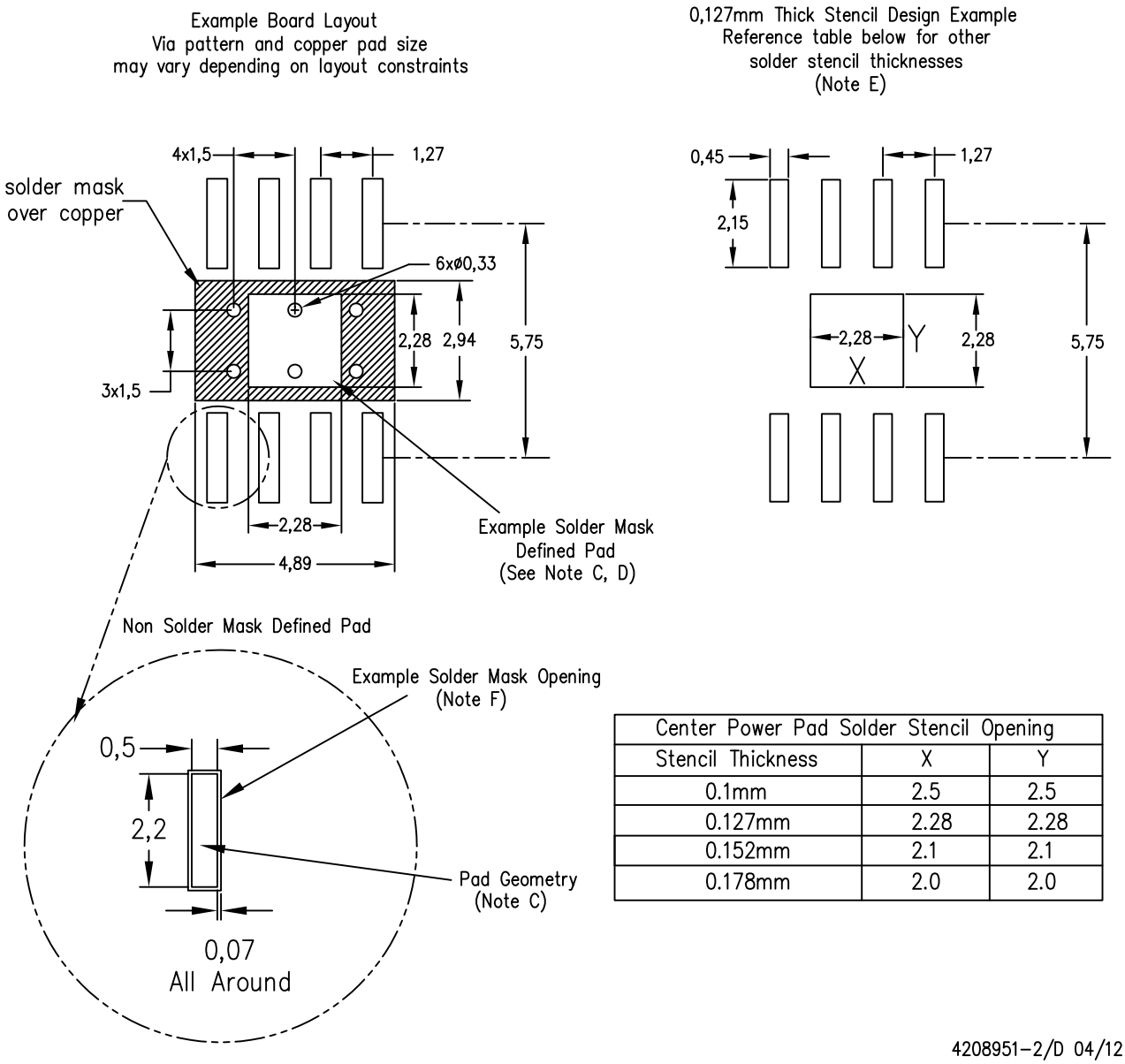
Exposed Thermal Pad Dimensions

4206322-2/L 05/12

NOTE: A. All linear dimensions are in millimeters

PowerPAD is a trademark of Texas Instruments

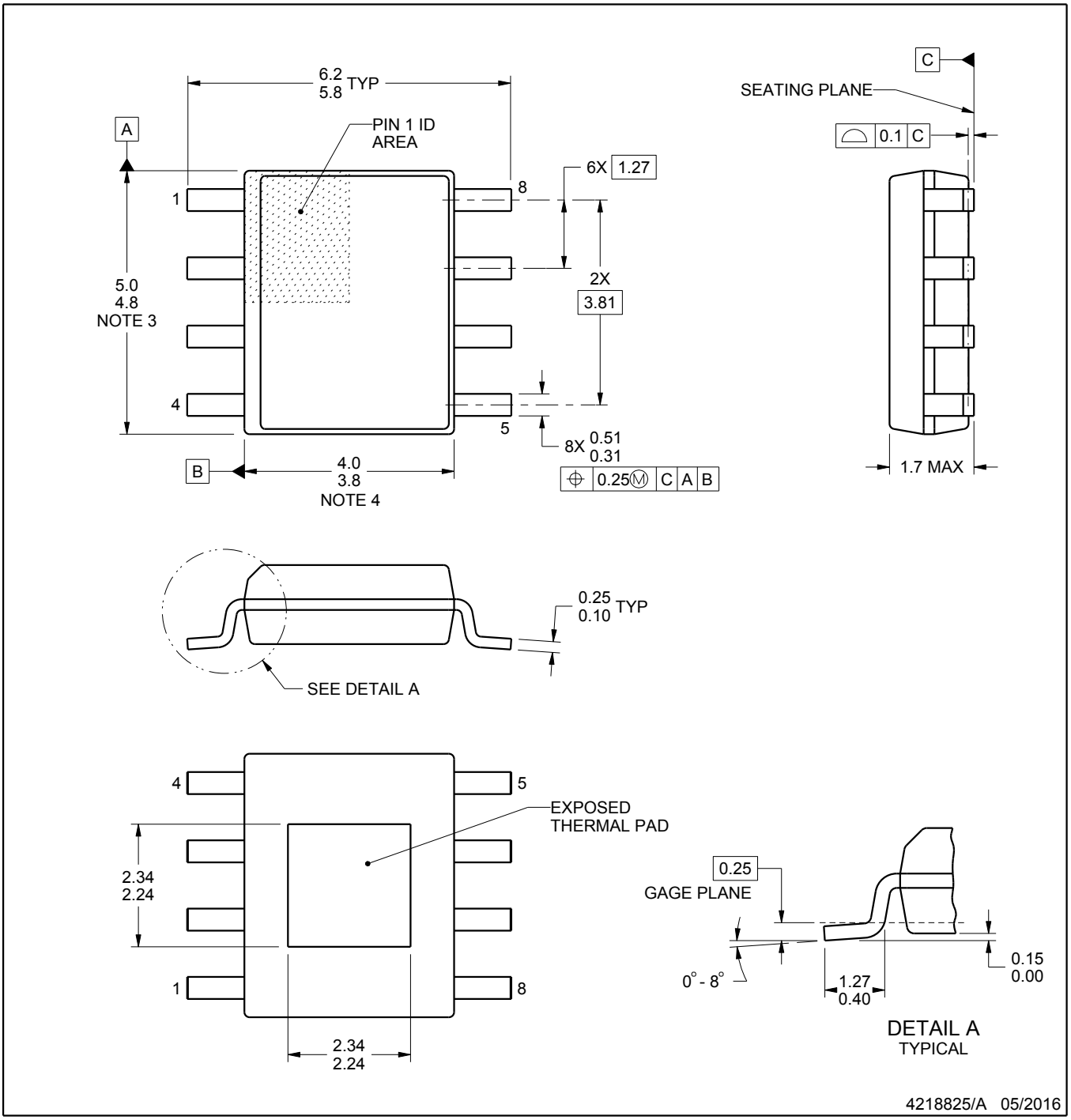
DDA (R–PDSO–G8) PowerPAD™ PLASTIC SMALL OUTLINE



Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	2.5	2.5
0.127mm	2.28	2.28
0.152mm	2.1	2.1
0.178mm	2.0	2.0

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

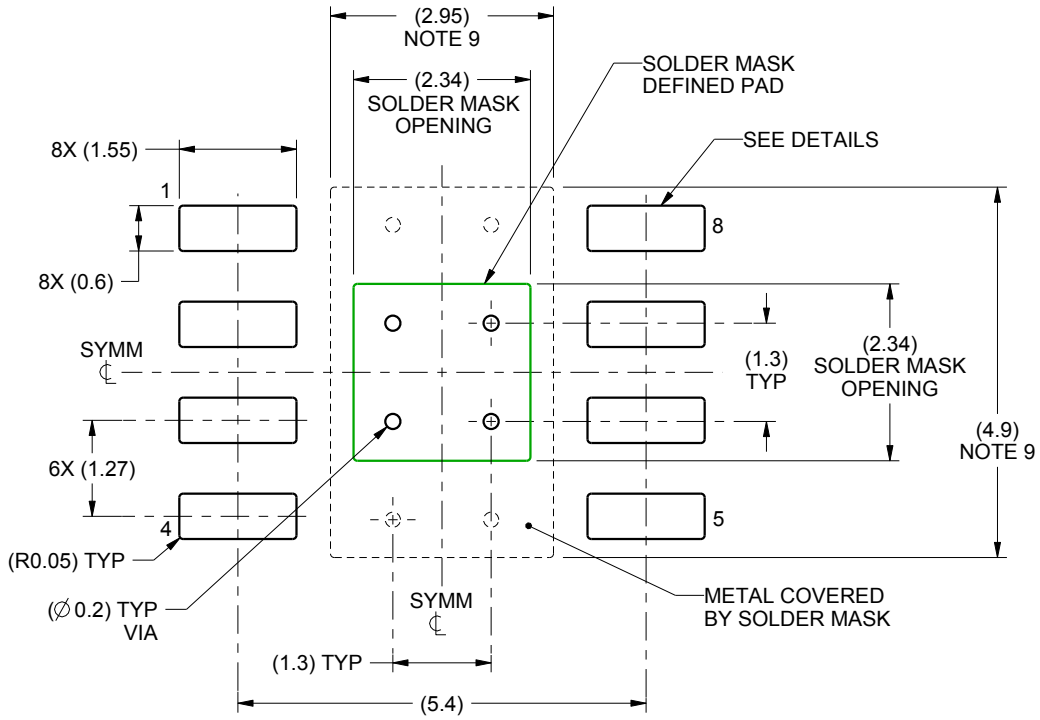
PowerPAD is a trademark of Texas Instruments.



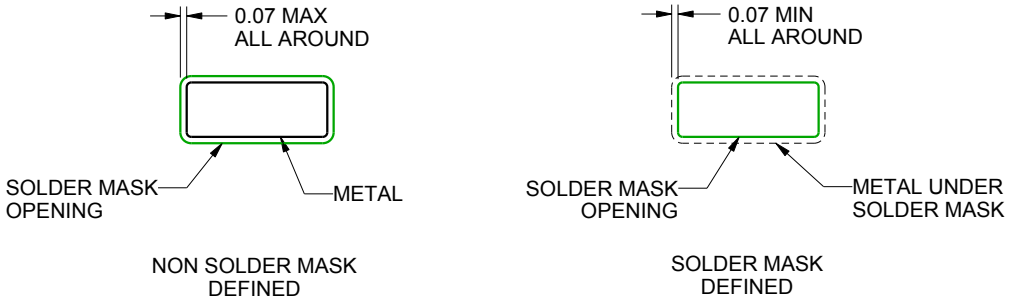
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MS-012.



LAND PATTERN EXAMPLE
SCALE:10X

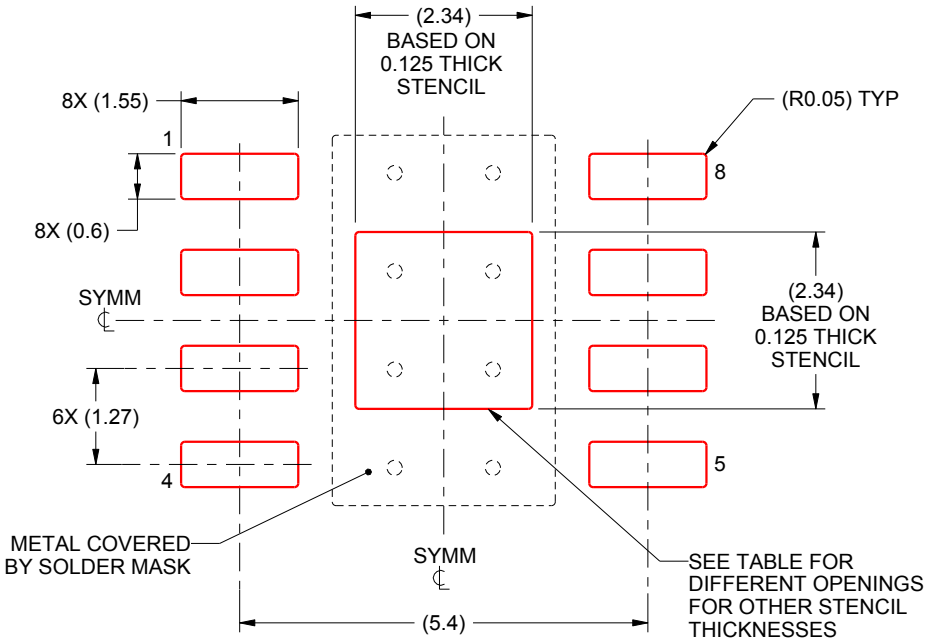


SOLDER MASK DETAILS

4218825/A 05/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.
10. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



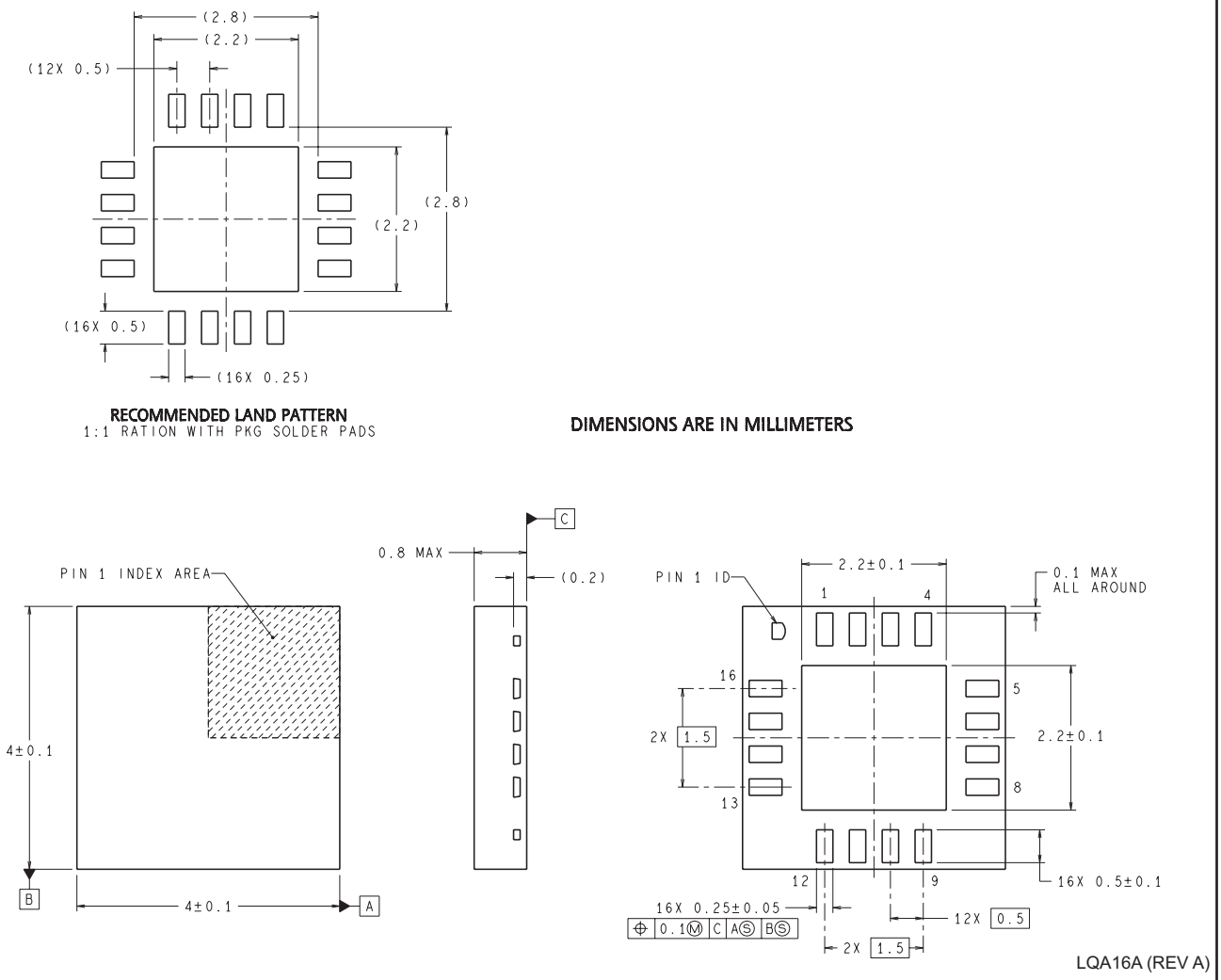
SOLDER PASTE EXAMPLE
EXPOSED PAD
100% PRINTED SOLDER COVERAGE BY AREA
SCALE:10X

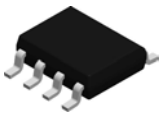
STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	2.62 X 2.62
0.125	2.34 X 2.34 (SHOWN)
0.150	2.14 X 2.14
0.175	1.98 X 1.98

4218825/A 05/2016

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.


(2.8)
(2.2)
(12X 0.5)
(2.8)
(2.2)
(16X 0.5)
(16X 0.25)
RECOMMENDED LAND PATTERN
1:1 RATION WITH PKG SOLDER PADS
DIMENSIONS ARE IN MILLIMETERS
C
0.8 MAX
(0.2)
PIN 1 INDEX AREA
4±0.1
B
4±0.1
A
PIN 1 ID
2.2±0.1
0.1 MAX
ALL AROUND
1
4
16
5
2X 1.5
2.2±0.1
13
8
12
9
16X 0.5±0.1
16X 0.25±0.05
0.1 M C A S B S
12X 0.5
2X 1.5
LQA16A (REV A)

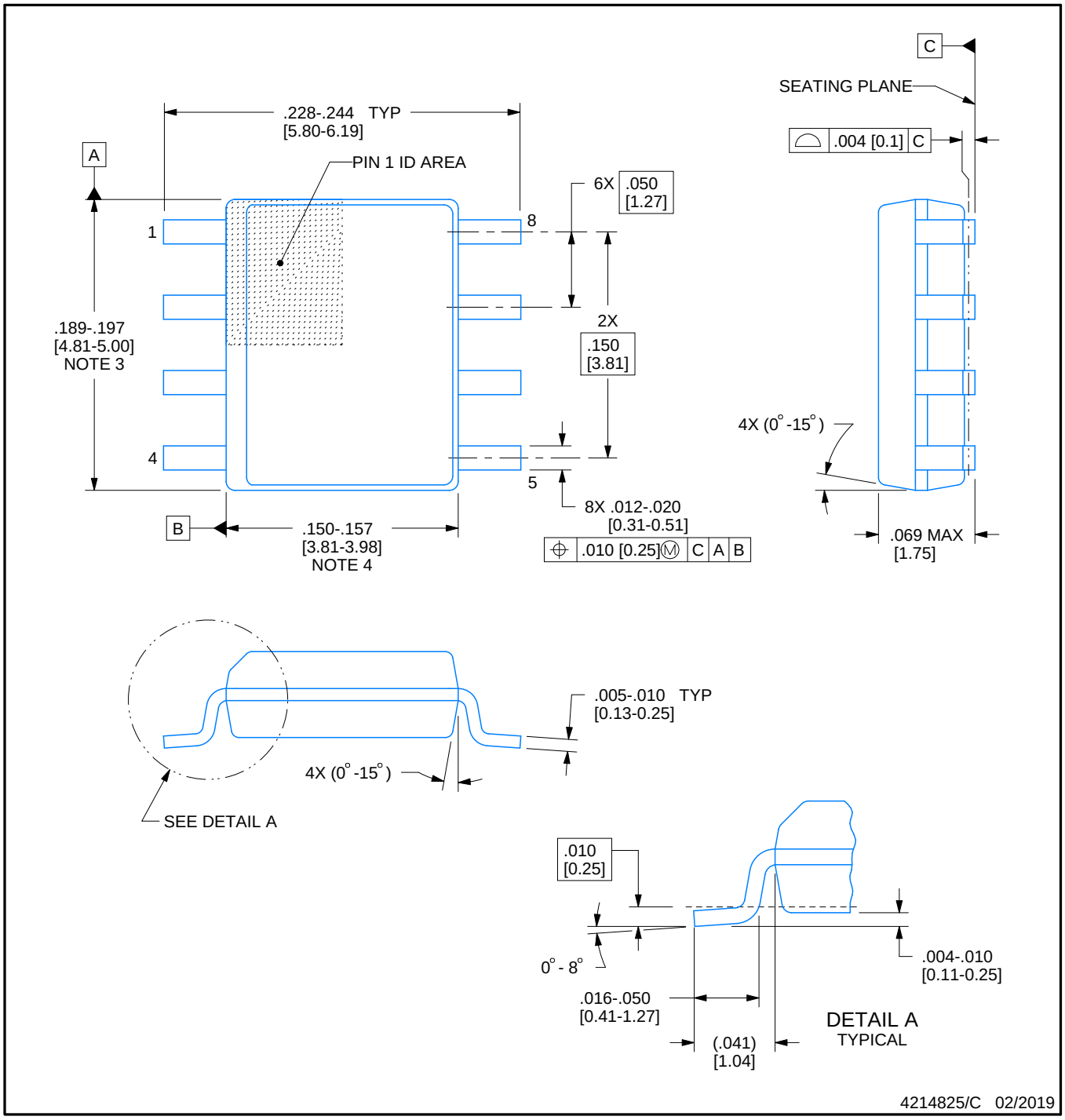


PACKAGE OUTLINE

D0008A

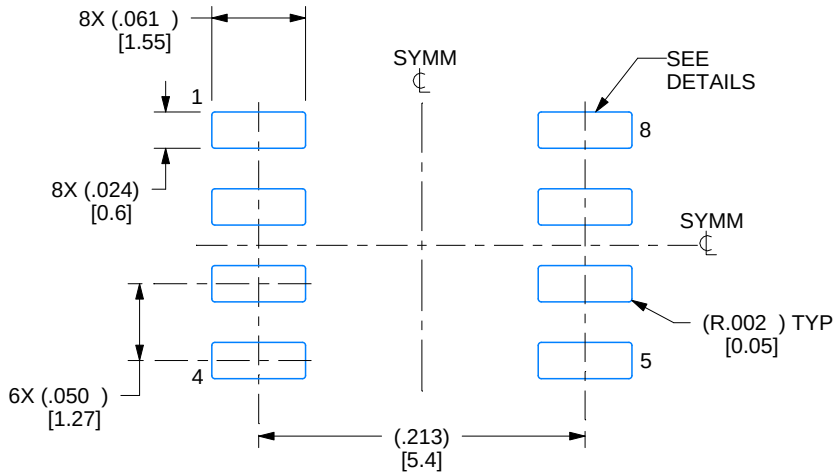
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

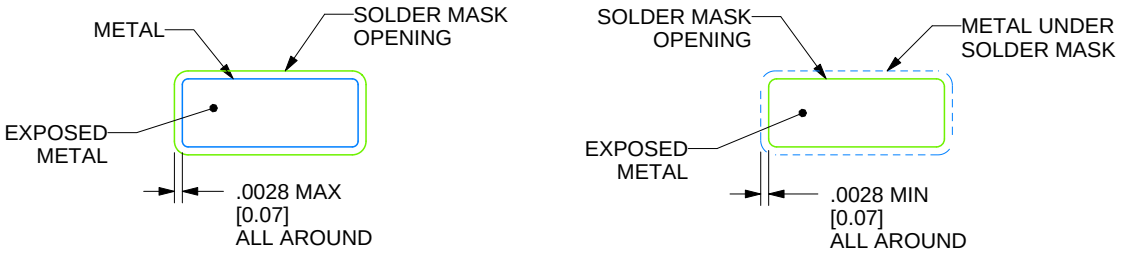


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

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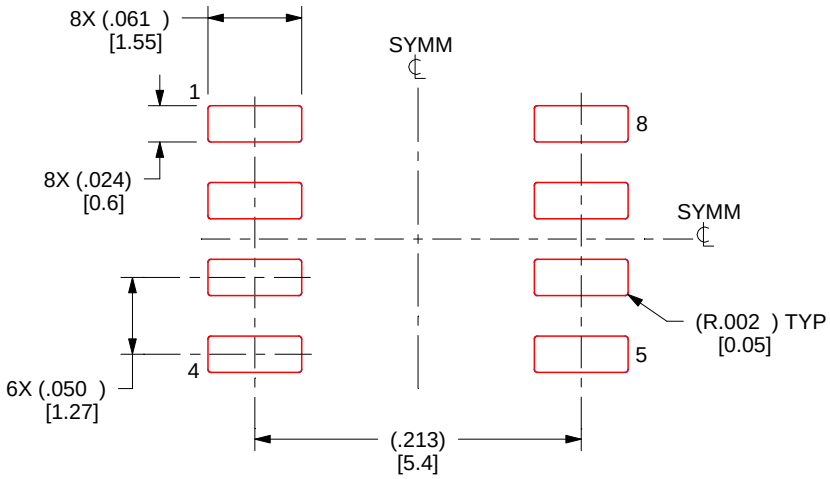
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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